High-Speed GaAs Static Random-Access Memory

GEORGES BERT, JEAN-PAUL MORIN, GERARD NUZILLAT, AND CHRISTIAN ARNODO

Abstract—An 8-bit fully decoded RAM test circuit has been designed and fabricated using enhancement-mode GaAs-MESFET's with the LPFL circuit approach. Correct operation of the circuit has been observed for a supply voltage varying from 3.5 to 7 V. An access time of 0.6 ns was measured for a total power consumption of 85 mW under nominal operating conditions. This circuit was used to develop and validate both a design strategy and computer-aided design (CAD) tools oriented towards cache or buffer memories of realistic complexity. It is shown that a performance-optimized 1-kbit RAM exhibiting an access time of 1.1 ns for a power dissipation of 850 mW would be feasible with the present fabrication technology.

I. Introduction

MOST applications of gallium arsenide integrated circuits in future high-performance digital systems, such as computers and detection or communication systems, will require memory circuits with speed compatible with that of GaAs logic IC's [1]. The principal utilization of these circuits could be buffer or cache memories and a complexity of 1-kbit, permitted by the present status of GaAs digital IC technology, appears to be acceptable for many high-speed digital processing requirements.

Development of GaAs RAM circuits is planned in several laboratories [2]–[4], but only two prototype realizations have been reported to date. A 16-bit RAM test circuit was fabricated by Asai *et al.* who measured an access time of 10 ns for a power consumption of 2 mW [5]. We have reported recently an access time measurement of 0.6 ns for a 8-bit fully decoded RAM prototype with a power consumption of 85 mW [6]. This circuit was intended to serve the dual purpose of showing the feasibility of subnanosecond memory based on GaAs technology, and of developing the computer-aided design (CAD) tools necessary to extend the results obtained with the prototype circuit to larger GaAs random access memories.

In this paper, the design, fabrication, and performances of this first subnanosecond access time RAM circuit are described in detail. Based on the experimental results obtained, the optimized circuit design of a 1-kbit GaAs RAM circuit is presented and its expected performance is discussed assuming the same design rules and fabrication parameters.

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II. Circuit Approach and Fabrication Process

Since random-access memories are basically complex IC's, a circuit approach using enhancement-mode MESFET's should be preferred in order to optimize the power consumption. This is the reason why all the GaAs RAM designs reported to date are based on the conventional normally-off FET circuit approach, known as direct coupled FET logic (DCFL). In order to ensure more comfortable fabrication tolerances and improve circuit-design flexibility we have chosen, for the GaAs RAM design, our quasi-normally-off approach named low pinchoff-voltage FET logic (LPFL) [1] rather than the DCFL [7], [8]. Therefore, the acceptable range of pinchoff voltage was increased up to 0.5 V centered around 0.0 V.

The main features of the fabrication process are as follows.

1) VPE-grown active layers with a carrier concentration of $1\text{–}1.5\times10^{17}$ cm^{-3} were used. The sheet resistance was 1.5–2.5 kΩ/□. The device isolation was achieved either by mesa etching or deep boron implantation.

2) The pattern definition was obtained by combining direct-writing electron-beam lithography and lift-off technique. The MESFET gate length was 0.8 μm, whereas a 2-μm minimum line width was used for the two levels of interconnection.

3) Recessed-gate FET structures were used. The 1000-Å recess was made by 200-eV ion milling, followed by a flash chemical etching. The Ti/Pt/Au gate was annealed at 450°C for Schottky barrier characteristic stabilization ($\phi_B = 0.75$ V, $n = 1.05$). This routine ensures a pinchoff-voltage control within ±0.1 V.

III. 8-Bit Memory Design

The 8-bit RAM test circuit was designed under the following assumptions for the principal design parameters:

single supply voltage	$V_{DD} = 4.6$ V;
input logic swing	$\Delta V = 0.7$ V;
output drive capability	$I_{out} = 2$ mA into a 50-Ω load;
nominal pinchoff voltage	$V_p = 0.0$ V;
minimum transistor width	$Z_{min} = 20$ μm;
resistive loads	$R_\square = 2$ kΩ/□.

The circuit was organized into 4 words of 2 bits (4 rows

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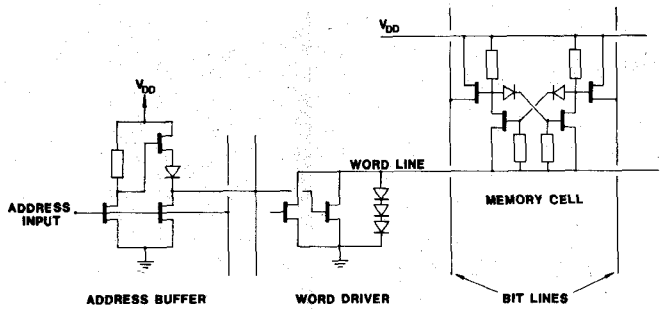

Fig. 1. Addressing scheme for the 4×2 RAM prototype.

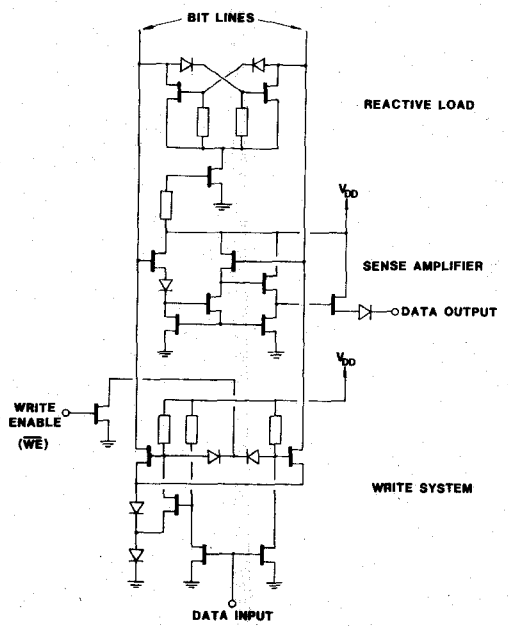

Fig. 2. Read and write systems for the 4×2 RAM prototype.

and 2 columns) with separate data inputs and outputs. Only a single 1-out-of-4 row decoder was required. The memory cell circuit diagram was deduced from the 3I-LPFL basic inverter configuration [8] and coupling with the bit lines was achieved in a novel way. Tradeoff considerations of the present approach and comparisons with previously proposed DCFL memory designs are discussed in Section V.

The basic memory cell given in Fig. 1 is rather complex (10 components per cell), but addition of Schottky diodes and pull-down resistors allows proper operation with large pinchoff-voltage tolerances. The novel access mode using common-drain MESFET's improves impedance matching between bit lines and internal nodes of the memory cell. With the minimum transistor width of 20 μm adopted in the actual circuit, the memory cell power consumption is about 2 mW.

The write operation is performed by drawing current through the gate of the access coupling transistor. This operation is achieved by the write circuitry shown in Fig. 2. Also shown in this figure is the read amplifier which uses a 2-stage totem-pole design to drive the output buffer transistor. It should be noted that the read system remains always active, and therefore the addressed cell content is available even during a write operation.

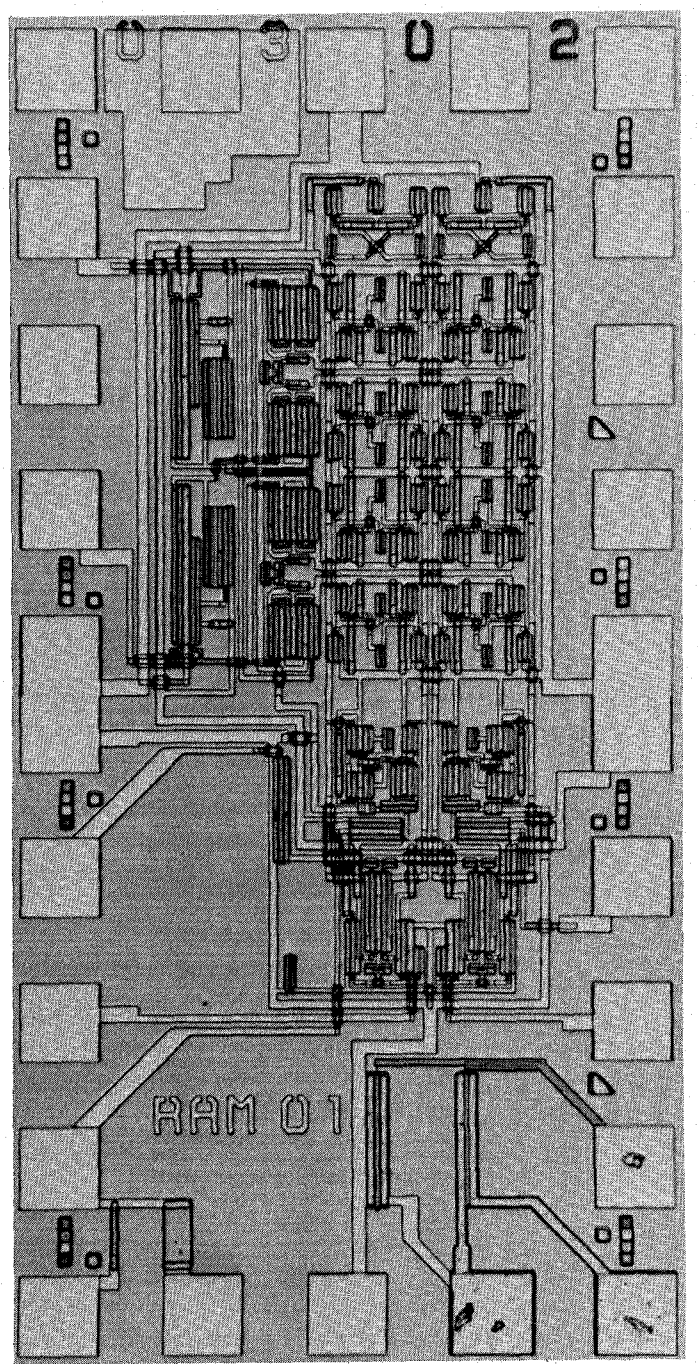

Fig. 3. Photomicrograph of the realized 4×2 RAM chip.

Fig. 3 shows a photomicrograph of the fabricated chip. The circuit dimensions including pads are 0.5 mm by 1 mm with an active area of 0.2 mm^2 for which 0.049 mm^2 comes from the 8-bit cell array, 0.038 mm^2 from the address system, and 0.035 mm^2 from the read and write circuitry. The basic memory cell area is 5900 μm^2. The circuit contains a total of 170 components including 77 MESFET's, 52 ohmic resistors, and 41 Schottky diodes. The memory cell matrix can be seen in the center of the photomicrograph and the address system is on the left-hand side. Both

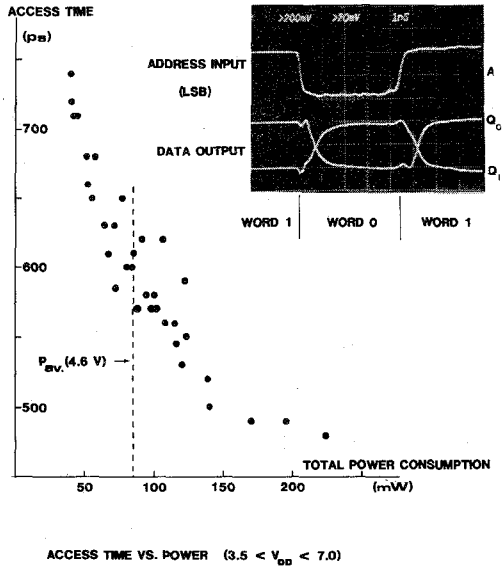

Fig. 4. Access time measurements on six 4×2 RAM circuits.

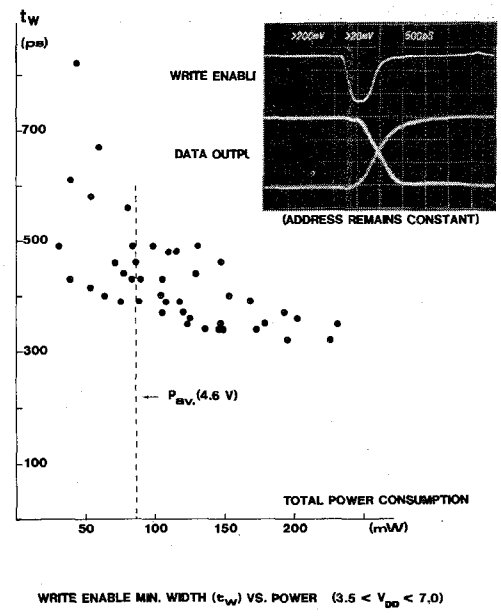

Fig. 5. Minimum write enable pulse width measurements on six 4×2 RAM circuits.

the read amplifier and the write circuitry with enable systems are located at the bottom.

IV. Circuit Performance Results

At the present time, 6 wafers have been processed and have exhibited quite similar results. The wafer-probe functional testing has led to a fabrication yield ranging between 10 percent (7/72) and 30 percent (22/72).

The access-time measurement results on the 6 best circuits taken out of 2 wafers are shown in Fig. 4. The supply voltage was varied from 3.5 to 7 V, for each chip, while maintaining correct operation of the circuit. The access time is defined as the elapsed time between an address change edge and the availability of the corresponding information on the output pads. The scope trace illustrates the read operation performed on 2 words. The mean power consumption for the standard supply voltage of 4.6 V is 85 mW, of which 15 mW are used by the output buffers. The corresponding measured access time is 600 ps. The minimum measured power consumption with 3.5 supply voltage is 40 mW. It is possible to obtain an access time lower than 500 ps with a supply voltage of 7 V.

In spite of the experimental difficulty involved, we have evaluated the minimum write-enable pulse width to allow a correct storage of the information. The dependence of this parameter on total power consumption, measured under the same conditions as those of access time, is shown in Fig. 5. The wide dispersion of experimental data is due to experimental errors rather than deviations in actual parameter values. At the nominal supply voltage, the measured minimum pulse width was found to range between 400 and 500 ps. This result, in conjunction with the access time measurements, demonstrates the capability of this 8-bit RAM test circuit to work properly up to a cycle frequency greater than 1.5 GHz.

Good agreement was observed between the experimental performances and computer simulations. By using the CIRCEC network analysis program[1], and assuming a typical set of parameter values, we have computed a simulated access time of 530 ps, which is in reasonable agreement with the measured data of 600 ps.

V. 1-kbit RAM Performance Projections

A. Design

By taking advantage of the circuit approaches utilized in the 8-bit RAM prototype, we have tried to evaluate achievable performances of GaAs RAM circuits of realistic complexity. In order to optimize power consumption and number of circuit pads, the following minor assumptions in the basic logic operators and in the general characteristics of the memory have been made:

1) nominal pinchoff voltage of +0.1 V with an acceptable range of ±0.2 V;
2) minimum transistor width of 5 μm;
3) replacement of ohmic resistor loads by active loads realized by MESFET's of −0.4-V pinchoff voltage, 5-μm transistor width, and gate length chosen to give the desired current;
4) two separate supply voltages for the memory matrix and the surrounding circuitry;
5) $N \times 1$-bit memory organization using a square matrix with row and column decoders.

The other design rules and fabrication parameters have not been changed.

The DCFL approach leads to the simplest memory cell and to the lowest power consumption. But a strictly positive and well-controlled pinchoff voltage is required to achieve acceptable noise immunity, especially for low-power RAM design. In spite of a more complex design, the LPFL

[1]Interactive nonlinear network analysis program developed by Thomson-CSF/DIS.

TABLE I
COMPARISON BETWEEN DCFL AND LPFL FLIP-FLOPS

	Number of components	Minimum supply voltage (V)	Logic swing (V)	Minimum pinchoff voltage (V)
DCFL	6	1	0.5	0
LPFL	10	1.6	1.1	-0.1

TABLE II
COMPARISON OF DIFFERENT MEMORY CELL COUPLING METHODS

	Number of access lines	Supply voltage (V)	Address current supplied by memory cell	Symetrical write	read current supplied by flip-flop
Switching FET	5	2.5	NO	YES	YES
Diode	4	3.7	YES	NO	YES
Common drain FET	4	3.7	YES	NO	NO

memory cell offers the advantage of a wider acceptable pinchoff voltage range [7] and a higher logic swing (1.1 V). (See Table I.)

Three coupling modes between the memory cell and the bit lines are compared in Table II. The common-drain FET coupling mode is chosen since it exhibits the advantage of allowing an impedance matching between the bit lines and the internal nodes of the cell. The write operation is performed by drawing current through the gate of the access coupling transistor.

The chosen electrical scheme for the row decoder compatible with the memory matrix is shown in Fig. 6. The propagation delay and the dimension of the word drivers depend on the memory-cell power consumption. CIRCEC simulations show that an optimum partition of power between matrix and row decoders can be found for a given total consumption, as seen in Fig. 7. This total consumption represents between 1/4 and 3/4 of the chip's consumption, depending on the circuit complexity and the power objective.

In order to improve the dynamic performance, a precharge system is connected to the bit lines (Fig. 8). This solution presents a disadvantage in terms of circuit complexity and requires one more signal input for the read operation, but allows a significant improvement in the speed performance.

The read system is implemented by connection of a sense amplifier on every matrix column and a further selection of a logical level by means of the column decoder. Special interface requirements have not been taken into consideration in the evaluation presented here. Details of the output circuitry depend on the particular application, and different designs can be utilized with the same memory

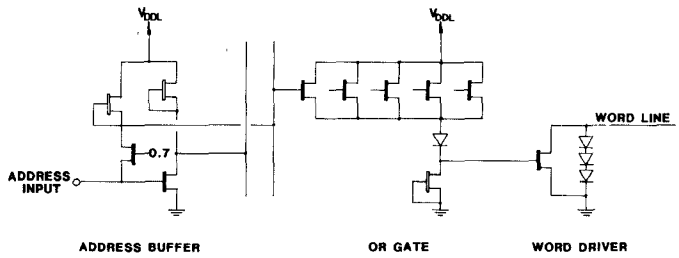

Fig. 6. Addressing scheme for 1-kbit RAM.

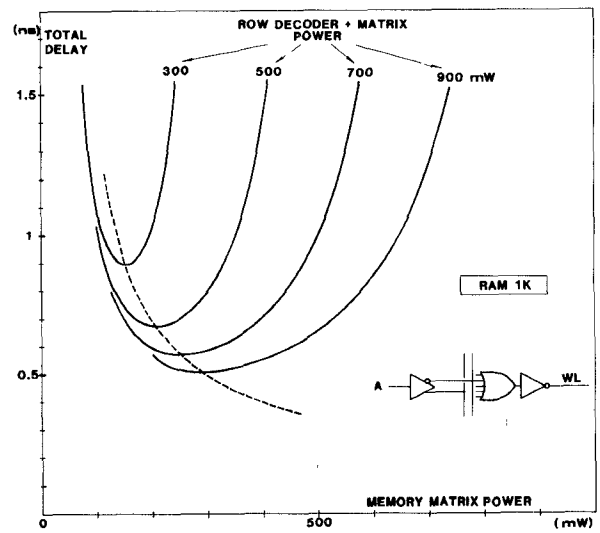

Fig. 7. Effect of the power consumption partition on the addressing delay (row decoder + word-drivers).

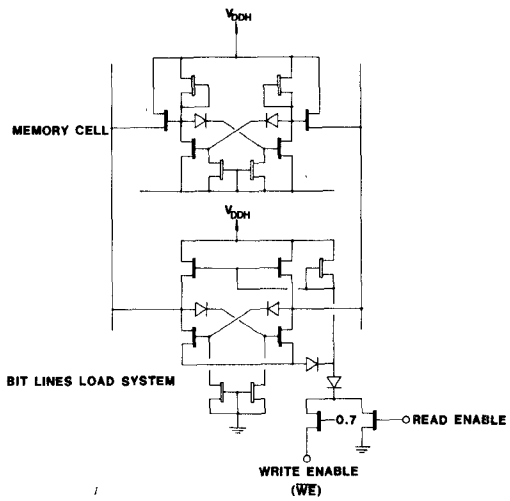

Fig. 8. E/D-LPFL memory cell and precharge system for 1-kbit RAM ($\simeq$ 0.2 mW/cell).

circuit. Propagation delay and power consumption of the interface circuitry should be added to the results presented in Tables III and IV. The output circuits considered are able to drive a 50-Ω line with 100–200-mV swing or higher impedance (500 Ω) with 0.7–1 V.

The propagation delay of the write system is not a significant parameter, since it only affects the delay between the address signals and the write signal (setup-time). This delay must be shorter than the address delay (row

TABLE III
"POWER BUDGET" FOR 256 AND 1-KBIT PROJECTS (SIMULATION)

	RAM 256 x 1-bit		
	Power consumption (mW)	Propagation delay (ns)	Access time (ns)
Y row decoder	365	0 19	0 65
Memory matrix	135	0 15	
Precharge circuits	44	0 12	
Sense amplifiers	79	0 19	
Write system	57	0 33	
X column decoder	50	0 34	
	730		
	RAM 1 K x 1-bit		
Y row decoder	290	0 33	1 08
Memory matrix	210	0 35	
Precharge circuits	54	0 15	
Sense amplifiers	155	0 25	
Write system	46	0 64	
X column decoder	100	0 40	
	855		

TABLE IV
MAIN FEATURES OF 64, 256, AND 1-KBIT PROJECTS (SIMULATION 0.2 MW/CELL)

	Access time (ns)	Total power consumption (mW)	Circuit area (mm^2)	Complexity (# components)
64 x 1	0 85	140	0 7	1100
256 x 1	0 95	200	1 8	3500
1024 x 1	1 1	850	5 0	12000

decoder + word drivers) in order to avoid an increase in the memory cycle time. The minimum write-enable pulse width (t_w) corresponds to the switching time of the memory cell and is not an actual limitation for speed performance of memories with complexities up to 1 kbit ($\simeq 800$ ps for 1 kbit).

The column decoder propagation delay must be shorter than the row addressing time (row decoder + word drivers) and its power consumption can be reduced to a lower value than that of the row decoder.

B. Performance Projections

The characteristics presented hereafter have been calculated under the general assumptions and design strategy presented in part *A* of this section. Other chosen parameter values are as follows:

supply voltages	+3.9 V and +2.5 V;
memory cell dimensions	50 μm × 50 μm;
width of coupling FET	10 μm to 20 μm (depending on complexity);
enhancement-mode FET current	130 μA ($Z = 5$ μm, $V_p = +0.1$ V);
parasitic capacitances	2×10^{-3} pF per crossover; 8×10^{-5} pF/μm for crosstalk.

The speed and power performance for both 256-bit and 1-kbit RAM circuits are given in detail in Table III. A total power consumption of about 800 mW was assumed, of which 500 mW were allocated to the memory matrix plus the row decoder. The speed–power performance was optimized by using the information available from the curves in Fig. 7 to partition the power between the row decoder and the cell array. For the 1-kbit circuit, the corresponding stand-by power dissipation is 0.2 mW/cell. It appears that an access time as low as 650 ps can be anticipated for the 256-bit circuit, and that the 1-kbit RAM should exhibit an access time of 1.1 ns, corresponding to the very attractive figure of merit of 0.92 pJ/bit. For comparison purposes, it can be noted that a 1-kbit circuit design, assuming no precharge and a power dissipation of 0.45 mW/cell, has led to an access time of 1.6 ns with a total power consumption of 1.2 W [6].

The projected characteristics of three RAM circuits of increasing complexity are listed in Table IV. The same optimization method was used, but the stand-by power consumption was now assumed to be constant, with a value of about 0.2 mW/cell. The power consumption of the 256-bit circuit is thus drastically reduced, but at the expense of speed.

VI. CONCLUSIONS

The 8-bit fully decoded RAM test circuit presented in this paper demonstrates the feasibility of subnanosecond access-time memories utilizing enhancement-mode GaAs MESFET's. A rather complex cell design has been chosen, (10 components per cell) using a new coupling mode with the bit lines in order to reduce increase noise immunity and the sensitivity to pinchoff-voltage variations. The preliminary data of fabrication yield, as well as the observed wide range of supply voltage allowing correct operation (3.5 to 7 V), validate this approach.

A computer analysis of the performance of RAM's with realistic complexities in cache or buffer memory application has been carried out in order to optimize the design and to predict the achievable speed–power performance. It has been shown that access-time reduction requires bit-line precharge and that the power sharing between cell array and row decoder is a very important consideration in speed optimization. Especially, it has been demonstrated that, with the cell design presently used, the maximum speed of 1-kbit RAM is obtained by consuming about 25 percent of the total power in the cell array (200 μW/cell). Under this condition, it has been shown that a 1-kbit RAM with an access time of 1.1 ns and a power dissipation of 850 mW would be feasible with only minor changes in the design parameters and the fabrication process.

The design strategy presented in this paper is certainly valid for RAM's of complexities up to 4-kbit, which covers most applications of fast memories in presently planned GaAs-implemented high-speed digital systems. For applications requiring larger memory sizes, 16-kbit or more, the memory cell will have to be redesigned in order to drastically reduce the standby power consumption. Such circuit complexities are well beyond the present status of GaAs IC technology.

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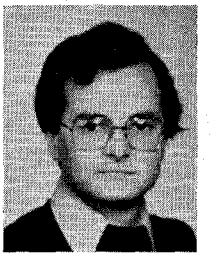

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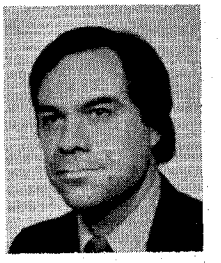

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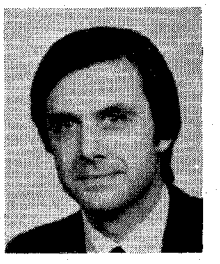

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